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EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/430,192	Applicant(s) RAYNHAM ET AL.	
	Examiner Tonia L Meonske	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *30 July 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction filed on July 30, 2002 has been disapproved because it is not in the form of a pen-and-ink sketch showing changes in red ink or with the changes otherwise highlighted. See MPEP § 608.02(v).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Page, Ian "The Harp Reconfigurable Computing System," Oxford University Hardware Compilation Group, October 1994 (herein referred to as Page).

4. Referring to claim 6, Page has taught a method for controlling a subsystem within a complex electrical device, the method comprising:

a. providing a single-IC subsystem controller (page 1, section 1.0, the microprocessor, the dynamic RAM, static RAM, frequency synthesizer, and parallel expansion port work together to control the Xilinx 3195 Field Programmable Gate Array, which is a single-IC subsystem (page 3, section 3, paragraph 2));

b. programming control functionality into the single-IC subsystem controller by:

i. programming logic circuits into a complex programmable logic device included in the single-IC subsystem controller (Page page 1, bullet "Xilinx 3195 Field Programmable Gate Array");

ii. implementing software routines for execution by a micro-controller within the single-IC subsystem controller (Page page 1, paragraph 3, bullet "32-bit RISC-style microprocessor" and page 2, paragraph 2, The microprocessor within the single-IC subsystem controller executes software routines.); and

iii. storing the software routines in the single-IC subsystem controller (Page page 1, bullet "4 Mbytes of dynamic RAM", The software routines are stored in the RAM, which is in the single-IC subsystem controller.); and

c. interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device (Page page 4, section 3.1, the frequency synthesizer generates a clock signal for the FPGA, so the FPGA, or subsystem, is connected to the single-IC subsystem controller.).

5. Referring to claim 8, Page has taught the method wherein the complex electrical device is a computer system (Page title "The HARP Reconfigurable Computing System").

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 4, 5, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Page, Ian "The Harp Reconfigurable Computing System," Oxford University Hardware Compilation Group, October 1994 (herein referred to as Page) in view of Pfaffenberger, Ph.D., Bryan, Que's Computer User's Dictionary, 5th Ed., 1994 (herein referred to as Que).

8. For the purposes of Examiner's prior art rejection of claim 1, the limitation "system processing components" will be assumed to denote the main processor or other components of the overall computer system as connected by a bus interface to the subsystem controller. Please see the 112-2nd paragraph rejection of this claim above.

9. Referring to claim 1, Page has taught a subsystem controller implemented as a single integrate circuit for control of a device of a subsystem within an electronic system having system processing components, the subsystem controller comprising:

a. a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality (Page page 1, bullet "Xilinx 3195 Field Programmable Gate Array");

b. a micro-controller that can execute software routines that implement control functionality (Page page 1, bullet "32-bit RISC-style microprocessor");

c. memory that stores executable code for execution by the micro-controller (Page page 1, bullet "4Mbytes of dynamic RAM");

d. random-access memory that can store data and executable code for execution by the micro-controller (Page page 1, bullet "two independent banks of 32K x 16-bit fast static RAM)

e. a bus interface for exchanging data and control signals between the subsystem controller and system processing components (Page page 1, last bullet and page 4, section 3.1, paragraph 1); and

f. an additional electronic interface to a device or subsystem controlled by the subsystem controller (Page page 4, section 3.1, The FPGA is interfaced to the subsystem controller.).

Page has not explicitly taught the memory that stores executable code for execution by the micro-controller as read-only memory (ROM). However, Que has taught utilizing ROM in place of the random-access memory (RAM) to store executable code to be run on the micro-controller would have allowed for the system to retain such code in the system power-off state and load the code immediately upon a change to power-up (Que page 416). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize read-only memory, or ROM, to store executable code for execution by the micro-controller as taught by Que instead of the random-access memory, or RAM, of Page, in order to ensure immediate loading of the code upon system power-up.

10. Referring to claim 2, Page has taught the subsystem controller wherein control functionality of the subsystem controller is partitioned between logic circuits programmed into the complex programmable logic device and software routines executed by the micro-controller (Page page 2, paragraph 2).

11. Referring to claim 4, Page has taught the subsystem controller wherein the bus interface is an I^2C bus interface (Page page 1, last bullet and page 4, section 3.1, paragraph 1 where the connection of several HARP boards, which are single integrated circuit boards (ICs), must be by

way of I^2C, or inter-integrated circuit buses such that any bus connecting 2 integrated circuits is an I^2C bus).

12. Referring to claim 5, Page has taught the subsystem controller wherein the additional electronic interface is an 8-bit input/output bus and additional signal lines (Page page 4, section 3.1, paragraph 3 where the 20Mbit/sec links break down into an 8-bit bus and several additional lines making up the other bits).

13. Referring to claim 9, Page has taught the method wherein the single-IC subsystem controller includes the complex programmable logic device (Page page 1, bullet "Xilinx 3195 Field Programmable Gate Array"), the micro-controller (Page page 1, bullet "32-bit RISC-style microprocessor"), a random-access memory (Page page 1, bullet "two independent banks of 32K x 16-bit fast static RAM), a bus interface (Page page 1, last bullet and page 4, section 3.1, paragraph 1), and an additional electronic interface (Page page 4, section 3.1, paragraph 3). Page has taught using a random-access memory (RAM), rather than a read-only memory (ROM) to store code to be executed by the micro-controller (Page page 1, bullet "4Mbytes of dynamic RAM"). However, Que has taught utilizing ROM in place of random-access memory (RAM) to store executable code to be run on the micro-controller would have allowed for the system to retain such code in the system power-off state and load the code immediately upon a change to power-up (Que page 416). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to utilize read-only memory, or ROM, to store executable code for execution by the micro-controller as taught by Que instead of the random-access memory, or RAM, of Page, in order to ensure immediate loading of the code upon system power-up.

14. Referring to claim 10, Page has taught the method wherein interconnecting the single-IC subsystem controller to the subsystem within the complex electrical device further includes interconnecting the subsystem with the additional electronic interface (Page page 4, section 3.1, paragraph 3).

15. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Page, Ian "The Harp Reconfigurable Computing System," Oxford University Hardware Compilation Group, October 1994 (herein referred to as Page) in view of Pfaffenberger, Ph.D., Bryan, Que's Computer User's Dictionary, 5th Ed., 1994 (herein referred to as Que) and further in view of Sudo, U.S. Patent Number 6,047,198 (herein referred to as Sudo). Each limitation of claim 1, from which this claim depends, has been taught as discussed in the rejection of claim 1 above. Neither Page nor Que have taught the subsystem controller programmed to control the display of information on an LCD display window included in an external front panel display of a server computer. Sudo has taught a controller programmed to display information (Sudo figure 4, element 5A) on an LCD display window included in an external front panel display of a server computer (Sudo figures 3 and 4, element 5 and figures 8A-J). Sudo has further taught a general-purpose CPU (Sudo figure 4, element 7) to control the entire system. An artisan would have been motivated to employ the system of Page as the CPU of Sudo, where the complex programmable logic device is used as an input/output controller, in this case the LCD controller, such that these devices are especially suited to build the complex and error-prone device interfaces (Page page 2, paragraph 4). Furthermore, using the complex programmable logic device/micro-controller IC system would have allowed for less glue logic such that the LCD control would have been part of the overall system control, or CPU, rather than extra, external

circuitry. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to employ the IC subsystem controller of Page within the system of Sudo in order to decrease the amount of hardware required and make the overall system more cost-effective and lighter.

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Page, Ian "The Harp Reconfigurable Computing System," Oxford University Hardware Compilation Group, October 1994 (herein referred to as Page) in view of Sudo, U.S. Patent Number 6,047,198 (herein referred to as Sudo). Page has taught each limitation of claim 6, from which this claim depends, as discussed in the rejection of claim 6 above. Page has not taught the method wherein the subsystem is an LCD display window that displays information about the components within the complex electrical device and about the state of the complex electrical device. Sudo has taught a method including a complex electrical device, wherein a controller is programmed to display information (Sudo figure 4, element 5A) on a subsystem, i.e. an LCD display window (Sudo figures 3 and 4, element 5) that displays information about the components and state of the complex electrical device (Sudo figures 8A-J). Sudo has further taught a general-purpose CPU (Sudo figure 4, element 7) to control the entire system. An artisan would have been motivated to employ the system of Page as the CPU of Sudo, where the complex programmable logic device is used as an input/output controller, in this case the LCD controller, such that these devices are especially suited to build the complex and error-prone device interfaces (Page page 2, paragraph 4). Furthermore, using the complex programmable logic device/micro-controller IC system would have allowed for less glue logic such that the LCD control would have been part of the overall system control, or CPU, rather than extra, external circuitry. Therefore, it would have

been obvious to a person of ordinary skill in the art at the time the invention was made to employ the IC subsystem controller of Page within the system of Sudo in order to decrease the amount of hardware required and make the overall system more cost-effective and lighter.

Response to Arguments

17. Applicant's arguments filed July 30, 2002 have been fully considered but they are not persuasive.

18. On page 4, Applicant argues in essesnce :

"In independent claim 1, both the phrases "subsystem controller" and the term "single integrated circuit" clearly represent limitations."

However, in response to applicant's arguments, the recitation "subsystem controller implemented as a single integrated circuit" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

The body of the claim does not depend on the preamble for completeness, and the limitations in the body of the claim are able to stand alone. Also the preamble merely recites an intended use of the body of the claim. The intended use of the body of the claim could be in a subsystem controller in a single integrated-circuit. Therefore the preamble is not given any patentable weight.

19. On page 4-5, Applicant argues in essence :

"Applicants intended to claim in claims 1-10, and did, in fact, clearly claim a subsystem controller implemented as a single integrated circuit."

However, in claim 1, and also in depending claims 1-5, the subsystem controller implemented as a single integrated circuit is written in the preamble and is given no patentable weight, as described in the above arguments.

In claim 6 and depending claims 7-10, Applicant's did not claim a subsystem controller implemented as a single integrated circuit. Instead, Applicant's claimed "providing a single-IC subsystem controller. Examiner reads this limitation as a controller for a single-IC subsystem. See the rejections above for further clarification.

20. On pages 6-8, Applicant's argue in essence:

"Page's device is not a subsystem controller"

However, as described above in the rejections, the microprocessor, the dynamic RAM, static RAM, frequency synthesizer, and parallel expansion port work together to control the Xilinx 3195 Field Programmable Gate Array, or subsystem. Therefore Page's device is a subsystem controller.

21. On page 7-8, Applicant's argues in essence:

"Page does not disclose a single integrated-circuit implementation of any kind of device"

However on page 3, section 3, paragraph 2, page has disclosed that the FPGA is an integrated circuit,

22. On page 7, Applicant argues in essence :

"Sudo does not disclose a subsystem controller programmed to control display of information on an LCD display."

However, the LCD Driver (Element 5A of Figure 4) is a program which controls information displayed on the LCD. The CPU (Element 7 of Figure 4) is programmed

with the LCD driver to control display information on an LCD display, as seen in Figures 8a-j. (Column 4, lines 13-24) Sudo has in fact disclosed a subsystem controller programmed to control display of information on an LCD display.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
October 4, 2002

RICHARD L. ELLIS
PRIMARY EXAMINER